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(54) Method to form self-aligned gate structures and focus rings.

(57) A selective etching and chemical mechanical planarization process for the formation of self-aligned gate 15 and focus ring 19 structures surrounding an electron emission tip 13 for use in field emission displays in which the emission tip 13 is i) optionally sharpened through oxidation, ii) conformally deposited with a first layer 18, iii) deposited with a conductive layer 15, iv) deposited with a second insulating layer 14, v) deposited with a focus electrode ring layer 19, vi) optionally deposited with a buffering material 21, vii) planarized with a chemical mechanical planarization (CMP) step, to expose a portion of the second layer 14, viii) etched to form a self-aligned gate and focus ring 19, and thereby exposing the emitter tip 13, after which xi) the emitter tip 13 may be coated with a low work function material.

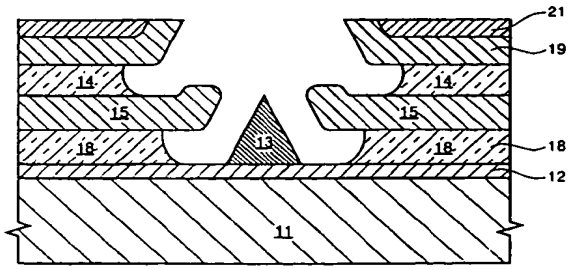

FIG. 7

EP 0 559 156 A1

Field of the Invention

This invention relates to field emission devices, and more particularly to processes for creating gate and focus ring structures which are self-aligned to the emitter tips using chemical mechanical planarization (CMP) and etching techniques.

Background of the Invention

Cathode ray tube (CRT) displays, such as those commonly used in desk-top computer screens, function as a result of a scanning electron beam from an electron gun, impinging on phosphors on a relatively distant screen. The electrons increase the energy level of the phosphors. When the phosphors return to their normal energy level, they release the energy from the electrons as a photon of light, which is transmitted through the glass screen of the display to the viewer.

Flat panel displays have become increasingly important in appliances requiring lightweight portable screens. Currently, such screens use electroluminescent or liquid crystal technology. A promising technology is the use of a matrix-addressable array of cold cathode emission devices to excite phosphor on a screen.

In U.S. Patent No. 3,875,442, entitled "Display Panel," Wasa et. al. disclose a display panel comprising a transparent gas-tight envelope, two main planar electrodes which are arranged within the gas-tight envelope parallel with each other, and a cathodoluminescent panel. One of the two main electrodes is a cold cathode, and the other is a low potential anode, gate, or grid. The cathode luminescent panel may consist of a transparent glass plate, a transparent electrode formed on the transparent glass plate, and a phosphor layer coated on the transparent electrode. The phosphor layer is made of, for example, zinc oxide which can be excited with low energy electrons.

Spindt, et. al. discuss field emission cathode structures in U.S. Patent Nos. 3,665,241, and 3,755,704, and 3,812,559, and 4,874,981. To produce the desired field emission, a potential source is provided with its positive terminal connected to the gate, or grid, and its negative terminal connected to the emitter electrode (cathode conductor substrate). The potential source may be made variable for the purpose of controlling the electron emission current. Upon application of a potential between the electrodes, an electric field is established between the emitter tips and the low potential anode grid, thus causing electrons to be emitted from the cathode tips through the holes in the grid electrode. This structure is depicted in Figure 1.

An array of points in registry with holes in low potential anode grids are adaptable to the production of cathodes subdivided into areas containing one or more tips from which areas emissions can be drawn separately by the application of the appropriate potentials thereto.

The clarity, or resolution, of a field emission display is a function of a number of factors, including emitter tip sharpness, alignment and spacing of the gates, or grid openings, which surround the tips, pixel size, as well as cathode-to-gate and cathode-to-screen voltages. These factors are also interrelated. Another factor which effects image sharpness is the angle at which the emitted electrons strike the phosphors of the display screen.

The distance (d) that the emitted electrons must travel from the baseplate to the faceplate is typically on the order of several hundred microns. The contrast and brightness of the display are optimized when the emitted electrons impinge on the phosphors located on the cathodoluminescent screen, or faceplate, at a substantially 90° angle. However, the contrast and brightness of the display are not currently optimized due to the fact that the initial electron trajectories assume a substantially conical pattern having an apex angle of roughly 30°, which emanates from the emitter tip. In addition, the space-charge effect results in coulombic repulsion among emitted electrons, which tends to further dispersion within the electron beam, as depicted in Figure 1.

U.S. Patent No. 5,070,282 entitled, "An Electron Source of the Field Emission Type," discloses a "controlling electrode" placed downstream of the "extracting electrode." U.S. Patent No. 4,943,343 entitled, "Self-aligned Gate Process for Fabricating Field Emitter Arrays," discloses the use of photoresist in the formation of self-aligned gate structures.

Summary of the Invention

The object of the present invention is to enhance image clarity on flat panel displays through the use of self-aligned gate and focus ring structures in the fabrication of cold cathode emitter tips. Chemical mechanical planarization (CMP) and selective etching techniques are key elements of the fabrication process.

The focus rings of the present invention, which are similar to the focusing structures of CRTs, function to collimate the emitted electrons so that the beam impinges on a smaller spot on the display screen, as seen in Figure 2.

One advantage of the process of the present invention is that it allows for the incorporation of focus rings into a cold cathode fabrication process, which provides enhanced collimation of electrons

emitted from the cathode emitter tips, and results in improved display contrast and clarity.

Another advantage of the process of the present invention is the fabrication of the focus rings is accomplished in a self-aligned manner, which greatly reduces process variability, and decreases manufacturing costs.

Brief Description of the Drawings

The process of the present invention will be better understood by reading the following description of nonlimitative embodiments, with reference to the attached drawings, wherein like parts in each of the several figures are identified by the same reference character, and which are briefly described as follows:

Figure 1 is a cross-sectional schematic drawing of a flat panel display showing a field emission cathode which lacks the self-aligned focus rings of the present invention;

Figure 2 is the flat panel display shown in Figure 1, further depicting the added focus ring structures of the present invention;

Figure 3 shows a field emission cathode, having a substantially conical emitter tip, on which has been deposited a first insulating layer, a conductive layer, a second insulating layer, a focus electrode layer, and a buffer layer according to the present invention;

Figure 3A shows the field emission cathode of Figure 3, further illustrating multiple insulating layers and focus electrode layers;

Figure 4 shows the multi-layer structure of Figure 3 after it has undergone chemical mechanical planarization (CMP), according to the present invention;

Figure 5 shows the structure of Figure 4, after a first etching, according to the present invention;

Figure 6 shows the structure of Figure 5, after a second etching, according to the present invention;

Figure 7 shows the structure of Figure 6, after etching, according to the present invention;

Figure 7A shows the structure of Figure 3A, after etching according to the present invention; and

Figure 8 is a flow diagram of the steps involved in the formation of self-aligned gate and focus-ring structures according to the present invention.

Detailed Description of the Invention

Referring to Figure 1, a field emission display employing a cold cathode is depicted. The substrate 11 can be comprised of glass, for example, or any of a variety of other suitable materials. In the preferred embodiment, a single crystal silicon layer serves as a substrate 11 onto which a conductive material layer 12, such as doped polycrystalline silicon has been deposited.

At a field emission site location, a micro-cathode 13 (also referred to herein as an emitter tip) has been constructed on top of the substrate 11. The micro-cathode 13 is a protuberance which may have a variety of shapes, such as pyramidal, conical, or other geometry which has a fine micro-point for the emission of electrons. Surrounding the micro-cathode 13, is a low potential anode gate structure 15.

When a voltage differential, through source 20, is applied between the cathode 13 and the gate 15, an electron stream 17 is emitted toward a phosphor coated screen 16. The screen 16 functions as the anode. The electron stream 17 tends to be divergent, becoming wider at greater distances from the tip of cathode 13.

The electron emission tip 13 is integral with the semiconductor substrate 11, and serves as a cathode conductor. Gate 15 serves as a low potential anode or grid structure for its respective cathode 13. A dielectric insulating layer 14 is deposited on the conductive cathode layer 12. The insulator 14 also has an opening at the field emission site location.

The cathode structure of Figure 2 is similar to Figure 1. However, beam collimating focus ring structures 19 fabricated by the process of the present invention, are also depicted. The focus rings 19 collimate the electron beam 17 emitted from each emitter 13 so as to reduce the area of the spot where the beam impinges on the phosphor coated screen 16, thereby improving image resolution.

The invention can best be understood with reference to Figures 3-8 of the drawings which depict the initial, intermediate and final structures produced by a series of manufacturing steps according to the invention.

There are several methods by which to form the electron emission tips 13 (Step A of Figure 8) employed in the process of the present invention. Examples of such methods are presented in U.S. Patent No.3,970,887 entitled "Micro-structure Field Emission Electron Source."

In practice, a P-type silicon wafer having formed therein (by suitable known doping pretreatment) a series of elongated, parallel extending opposite N-type conductivity regions, or wells. Each N-type conductivity strip has a width of approximately 10 microns, and a depth of approximately 3 microns. The spacing of the strips is arbitrary and can be adjusted to accommodate a desired number of field emission cathode sites to be formed on a given size silicon wafer substrate 11. (Processing

of the substrate to provide the P-type and N-type conductivity regions may be by any well-known semiconductor processing techniques, such as diffusion and/or epitaxial growth.) If desired, the P-type and N-type regions, of course, can be reversed through the use of a suitable starting substrate 11 and appropriate dopants.

The wells, having been implanted with ions will be the site of the emitter tips 13. A field emission cathode microstructure 13 can be manufactured using semiconductor substrate 11. The semiconductor substrate 11 may be either P or N-type and is selectively masked on one of its surfaces where it is desired to form field emission cathode sites. The masking is done in a manner such that the masked areas define islands on the surface of the underlying semiconductor substrate 11. Thereafter, selective sidewise removal of the underlying peripheral surrounding regions of the semiconductor substrate 11 beneath the edges of the masked island areas results in the production of a centrally disposed, raised, semiconductor field emitter tip 13 in the region immediately under each masked island area defining a field emission cathode site. It is preferred that the removal of underlying peripheral surrounding regions of the semiconductor substrate 11 be closely controlled by oxidation of the surface of the semiconductor substrate 11 surrounding the masked island areas with the oxidation phase being conducted sufficiently long to produce sideways growth of the resulting oxide layer beneath the peripheral edges of the masked areas to an extent required to leave only a non-oxidized tip 13 of underlying substrate 11 beneath the island mask. Thereafter, the oxide layer is differentially etched away at least in the regions immediately surrounding the masked island areas to result in the production of a centrally disposed, raised, semiconductor field emitter tip 13 integral with the underlying semiconductor substrate 11 at each desired field emission cathode site.

Before beginning the gate formation process, the tip 13 of the electron emitter may be sharpened through an oxidation process (Step A' of Figure 8). The surface of the silicon wafer (Si) 11 and the emitter tip 13 are oxidized to produce an oxide layer of SiO_2 (not shown), which is then etched to sharpen the tip 13. Any conventional, known oxidation process may be employed in forming the SiO_2, and etching the tip 13.

The next step (Step B of Figure 8) is the deposition of a insulating material 18 which is selectively etchable with respect to the conductive gate material 15. In the preferred embodiment, a silicon dioxide layer 18 is used. Other suitable selectively etchable materials, including but not limited to, silicon nitride and silicon oxynitride may also be used.

The thickness of this first insulating layer 18 will substantially determine both the gate 15 to cathode 13 spacing, as well as the gate 15 to substrate spacing 11. Hence, the insulating layer 18 must be as thin as possible, since small gate 15 to cathode 13 distances result in lower emitter drive voltages, at the same time, the insulating layer 18 must be large enough to prevent the oxide breakdown which occurs if the gate is not adequately spaced from the cathode conductor 12.

The oxide insulating layer 18, as shown in Figure 3, is preferably a conformal insulating layer. The oxide is deposited on the emitter tip 13 in a manner such that the oxide layer 18 conforms to the shape of the cathode emitter tip 13.

The next step in the process (Step C of Figure 8) is the deposition of the conductive gate material 15 (Figure 3). The gate 15 is formed from a conductive layer 15. The conductive material layer 15 may comprise a metal, such as chromium or molybdenum, but the preferred material for this process is deemed to be doped polysilicon or silicided polysilicon.

At this stage in the fabrication (Step D of Figure 8), a second insulating layer 14 is deposited (Figure 3). The second insulating layer 14 is substantially similar to the first insulating layer 18, e.g., layer 14 is also preferably conformal in nature. The second insulating layer 14 may also comprise silicon dioxide, silicon nitride, silicon oxynitride, as well as any other suitable selectively etchable material. The second insulating layer 14 substantially determines the gate 15 to focus ring 19 spacing (Figures 2 and 3).

The next process step (Step E of Figure 8), a focus electrode layer 19 is deposited (Figure 3). The focus rings 19 (Figure 2) will be formed from the focus electrode layer 19. The focus electrode material layer 19 is also a conductive layer which may be comprised of a metal, such as chromium or molybdenum, but as in the case with the conductive gate material layer 15, the preferred material is doped polysilicon or silicided polysilicon.

At this stage in the fabrication, (Step E'. of Figure 8) a buffer material 21 may be deposited to prevent the undesired etching of the lower-lying portions of the focus electrode material layer 19 during the chemical mechanical polishing (CMP) step (Step F of Figure 8) which follows. It should be emphasized that the deposition of a buffering layer 21 is an optional step.

A suitable buffering materials include a thin layer of Si_3N_4, or polyimide, or any other suitable buffering material known in the art. The nitride buffer layer 21 has the effect of enhancing the strength of the tip 13, which is one advantage of performing this optional step. The buffering layer 21 substantially impedes the progress of the CMP

into the layer on which the buffering material 21 is deposited.

The next step in the gate formation process (STEP F of Figure 8) is the chemical mechanical planarization (CMP), also referred to in the art as chemical mechanical polishing (CMP). Through the use of chemical and abrasive techniques, the buffer material as well as any other layers (e.g. the peaks of the focus electrode layer 19, the conformal insulating layers 14, 18, and the conductive gate layer 15) extending beyond the emitter tip 13 are "polished" away.

In general, CMP involves holding or rotating a wafer of semiconductor material against a wetted polishing surface under controlled chemical slurry, pressure, and temperature conditions. A chemical slurry containing a polishing agent such as alumina or silica may be utilized as the abrasive medium. Additionally, the chemical slurry may contain chemical etchants. This procedure may be used to produce a surface with a desired endpoint or thickness, which also has a polished and planarized surface. Such apparatus for polishing are disclosed in U.S. Patent Nos. 4,193,226 and 4,811,522. Another such apparatus is manufactured by Westech Engineering and is designated as a Model 372 Polisher.

CMP will be performed substantially over the entire wafer surface, and at a high pressure. Initially, CMP will proceed at a very fast rate, as the peaks are being removed, then the rate will slow dramatically after the peaks have been substantially removed. The removal rate of the CMP is proportionally related to the pressure and the hardness of the surface being planarized.

Figure 4 illustrates the intermediate step in the gate 15 formation process following the chemical mechanical planarization CMP. A substantially planar surface is achieved, and the second conformal insulating layer 14 is thereby exposed. At this point, (Step G of Figure 8) the various layers can be selectively etched to expose the emitter tip 13 and define the self-aligned gate 15 and focus ring 19 structures using any of the various etching techniques known in the art, for example, a wet etch. As a result of the CMP process, the order of layer removal can also be varied.

In the preferred embodiment, the second insulating layer 14 is selectively etched to expose the gate 15. Figure 5 shows the means by which the second conformal insulating layer 14 defines the gate 15 to focus ring 19 spacing, as well as the means by which the gate 15 and the focus rings 19 become self-aligned.

The gate material layer 15 is then etched, as shown in Figure 6. After the gate material layer 15 is removed, the first conformal insulating layer 18 which covers the emitter tip 13 is exposed.

The next process step is a wet etching of the first selectively etchable insulating layer 18 to expose the emitter tip 13. Figure 7 illustrates the field emitter device after the insulating cavity has been so etched.

In an alternative embodiment, (not shown) the gate material layer 15 can be removed first, thereby exposing the first insulating layer 18. Both of the selectively etchable insulating layers 14 and 18 can then be removed at the same time, thereby exposing the emitter tip 13.

If desired, the cathode tip 13 may optionally be coated with a low work function material (Step G' of Figure 8). Low work function materials include, but are not limited to cermet (Cr_3Si + SiO_2), cesium, rubidium, tantalum nitride, barium, chromium silicide, titanium carbide, molybdenum, and niobium.

Coating of the emitter tips may be accomplished in one of many ways. The low work function material or its precursor may be deposited through sputtering or other suitable means on the tip 13. Certain metals (e.g., titanium or chromium) may be reacted with the silicon of the tip to form silicide during a rapid thermal processing (RTP) step. Following the RTP step, any unreacted metal is removed from the tip 13. In a nitrogen ambient, deposited tantalum may be converted during RTP to tantalum nitride, a material having a particularly low work function.

The coating process variations are almost endless. This results in an emitter tip 13 that may not only be sharper than a plain silicon tip, but that also has greater resistance to erosion and a lower work function. The silicide is formed by the reaction of the refractory metal with the underlying polysilicon by an anneal step.

It is believed obvious to one skilled in the art that the manufacturing method described above is capable of considerable variation. For example, it is possible to fabricate several focus ring structures by adding successive insulating layers 14, 14a, etc., and conductive layers 19, 19a, etc. prior to the CMP step, (the relative level of the planarization step being indicated by the dotted line) and thereafter selectively etching the layers to expose the emitter tips 13, as shown in Figures 3A and 7A.

All of the U.S. Patents cited herein are hereby incorporated by reference herein as if set forth in their entirety.

While the particular process as herein shown and disclosed in detail is fully capable of obtaining the objects and advantages herein before stated, it is to be understood that it is merely illustrative of the presently understood embodiments of the invention and that no limitations are intended to the details of construction or design herein shown other than as described in the appended claims.

Claims

1. A process for the formation of self-aligned gate 15 and focus ring 19 structures around an electron emitter 13, said process comprising the following steps:
planarizing at least one electron emitter 13 overlaid with insulating 14, 18 and conductive layers 15, 19, said planarizing involving chemical mechanical means; and
selectively removing said insulating 14, 18 and conductive layers 15, 19, thereby exposing at least a portion of said electron emitter 13.

2. A process for the formation of multiple grid structures 15, 19 around an electron emitter 13, said process comprising the following steps:
forming at least one cathode 13 on a substrate 11;
forming at least two insulating layers 14, 18 superjacent said cathode 13;
depositing a conductive material layer 15, 19 superjacent each of said insulating layers 14, 18;
planarizing said layers 14, 15, 18, 19 by chemical mechanical planarization (CMP); and
removing said layers 14, 15, 18, 19 to expose at least a portion of said cathode 13.

3. A process for the formation of self-aligned gate 15 and focus ring 19 structures around an electron emitting tip 13, said process comprising the following steps:
forming at least one cathode 12 on a substrate 11, said cathode 12 having an emitter tip 13;
forming a first insulating layer 18 superjacent said emitter tip 13;
disposing a conductive layer 15 superjacent said first insulating layer 18;
disposing a second insulating layer 14 superjacent said conductive layer 15;
disposing a focus electrode layer 19 superjacent said second insulating layer 14;
polishing said layers 14, 15, 18, 19 to expose at least a portion of said conductive layer 15; and
selectively removing said layers 14, 15, 18, 19 to expose the emitter tip 13.

4. A process for the formation of self-aligned gate 15 and focus ring structures around a cathode emitter 13, said process comprising the following steps:
processing a wafer to form at least one cathode 12 on a substrate 11, said cathode having an emitter tip 13;
depositing a first insulating layer 18 upon said cathode 12;
depositing a conductive layer 15 superjacent said first insulating layer 18;
depositing a second insulating layer 14 superjacent said conductive layer 15;
depositing a focus electrode layer 19 superjacent said second insulating layer 14;
subjecting the wafer to chemical mechanical planarization (CMP) to expose at least a portion of said conductive material layer 15;
etching said layers 14, 18 to expose the emitter tip 13; and
coating said tip 13 with a material having a low work function.

5. A process for the formation of self-aligned gate 15 and focus ring 19 structures around a cathode tip 13, said process comprising the following steps:
forming at least one emitter tip 13 on a substrate 11;
depositing at least two insulating layers 14, 18 over said tip 13;
depositing at least two conductive layers 15, 19 superjacent said insulating layers 14, 18;
subjecting the wafer to chemical mechanical planarization (CMP), said chemical mechanical planarization being performed with an abrasive compound in a polishing slurry; and
etching said first and second insulating layers 14, 18 simultaneously thereby exposing the emitter tip 13.

6. A process for the formation of self-aligned gate 15 and focus ring 19 structures around an electron emitter 13, said process comprising the following steps:
processing a wafer to form at least one cathode 12 having an emitter tip 13;
sharpening said tip 13 by oxidation;
depositing a first insulating layer 18 over said tip 13;
depositing a conductive layer 15 superjacent said first insulating layer 18;
depositing a second insulating layer 18 superjacent said conductive layer 15;
depositing a focus electrode layer 19 superjacent said second insulating layer 14;
subjecting the wafer to chemical mechanical planarization (CMP) to expose at least a portion of said second insulating layer 14;
etching said second insulating layer 14 to create a cavity between said conductive layer 15 and said focus electrode layer 19;
etching said conductive layer 15 to form a

gate 15; and

removing a portion of said first insulating layer 18 surrounding the tip 13 thereby exposing said tip 13.

7. The process according to any of claims 1 to 6, wherein said first and second insulating layers 14, 18 are selectively etchable with respect to said conductive layer 15 and said focus electrode layer 19.

8. The process according to any of claims 1 to 6, further comprising the step of depositing a buffering layer 21 on said layer 19 prior to subjecting the wafer to the chemical mechanical planarization (CMP) step, said buffering material layer 21 comprising a thin layer of Si_3N_4.

9. The process according to any of claims 1 to 6, wherein said tip 13 is incorporated into an array of like tips 13 an optical display transmitter.

10. The process according to any of claims 1 to 6, wherein a plurality of said layers 19 and a plurality of said second insulating layers 14 are deposited.

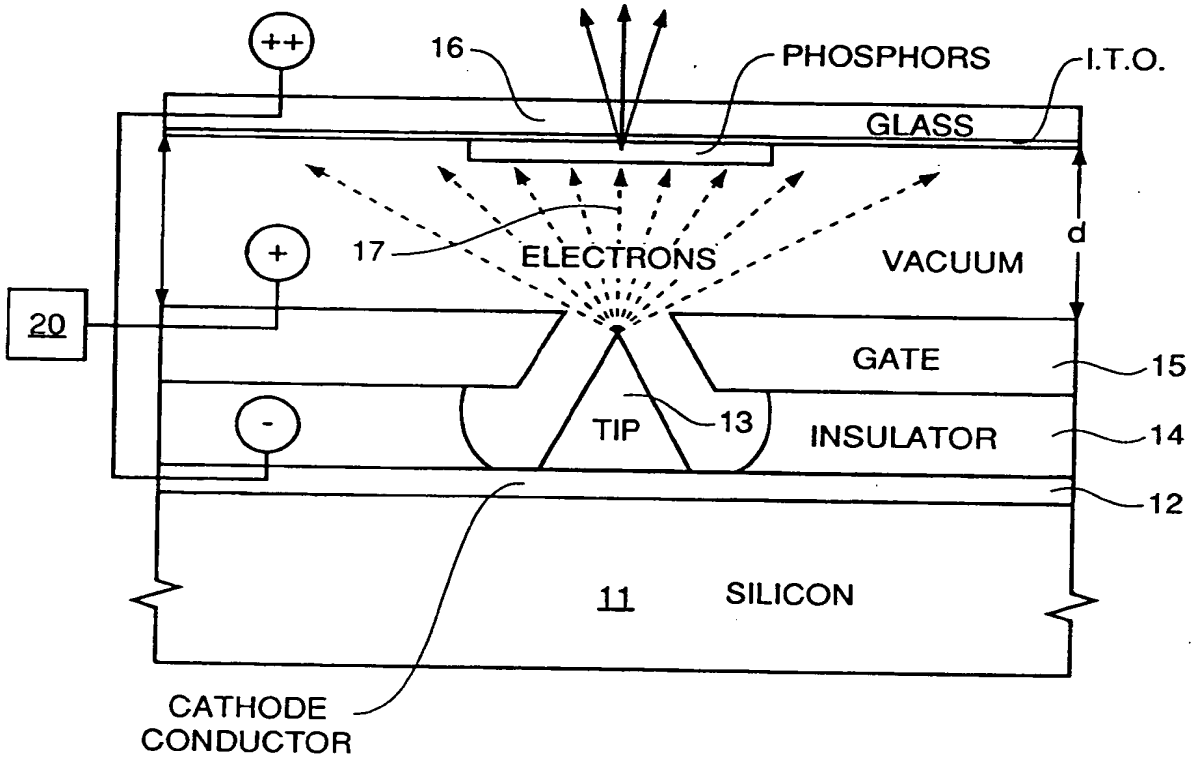
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FIG. 1

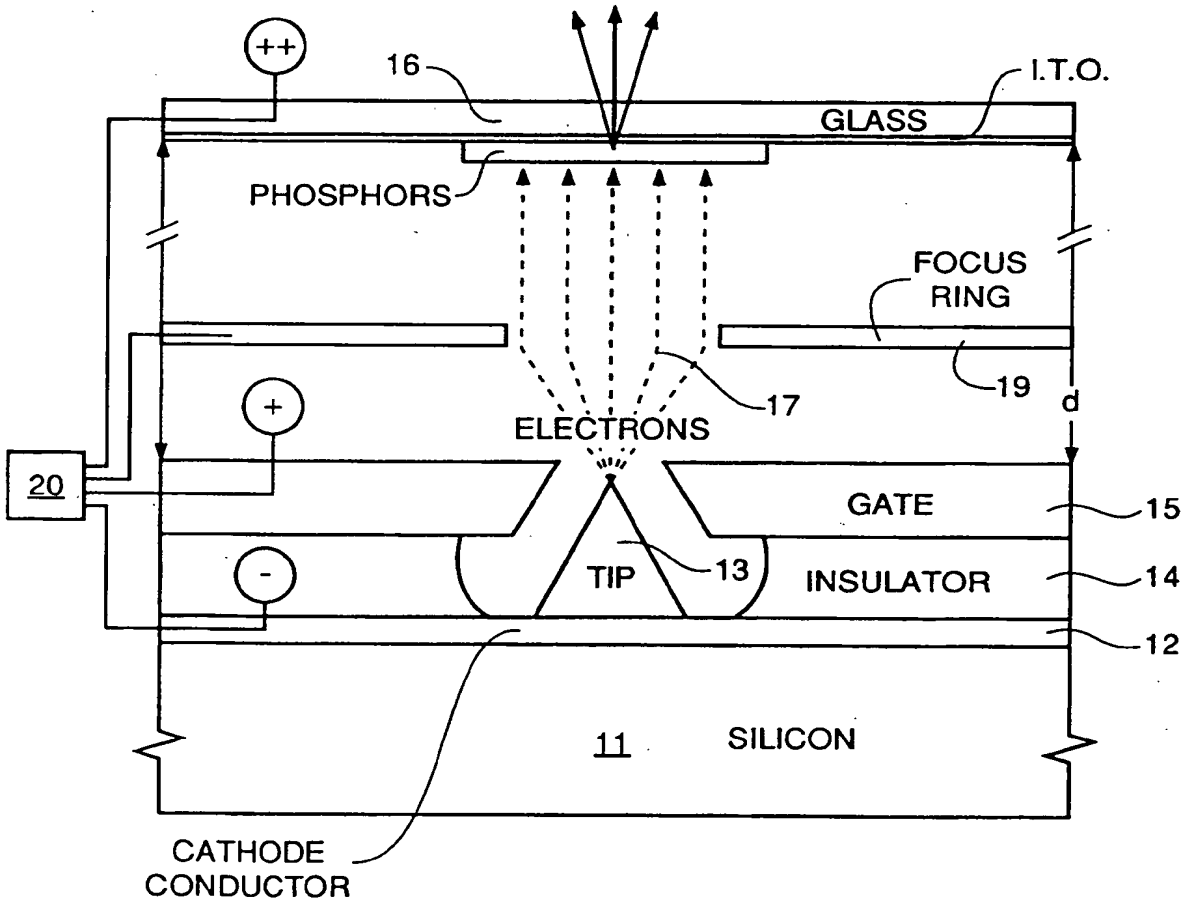
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FIG. 2

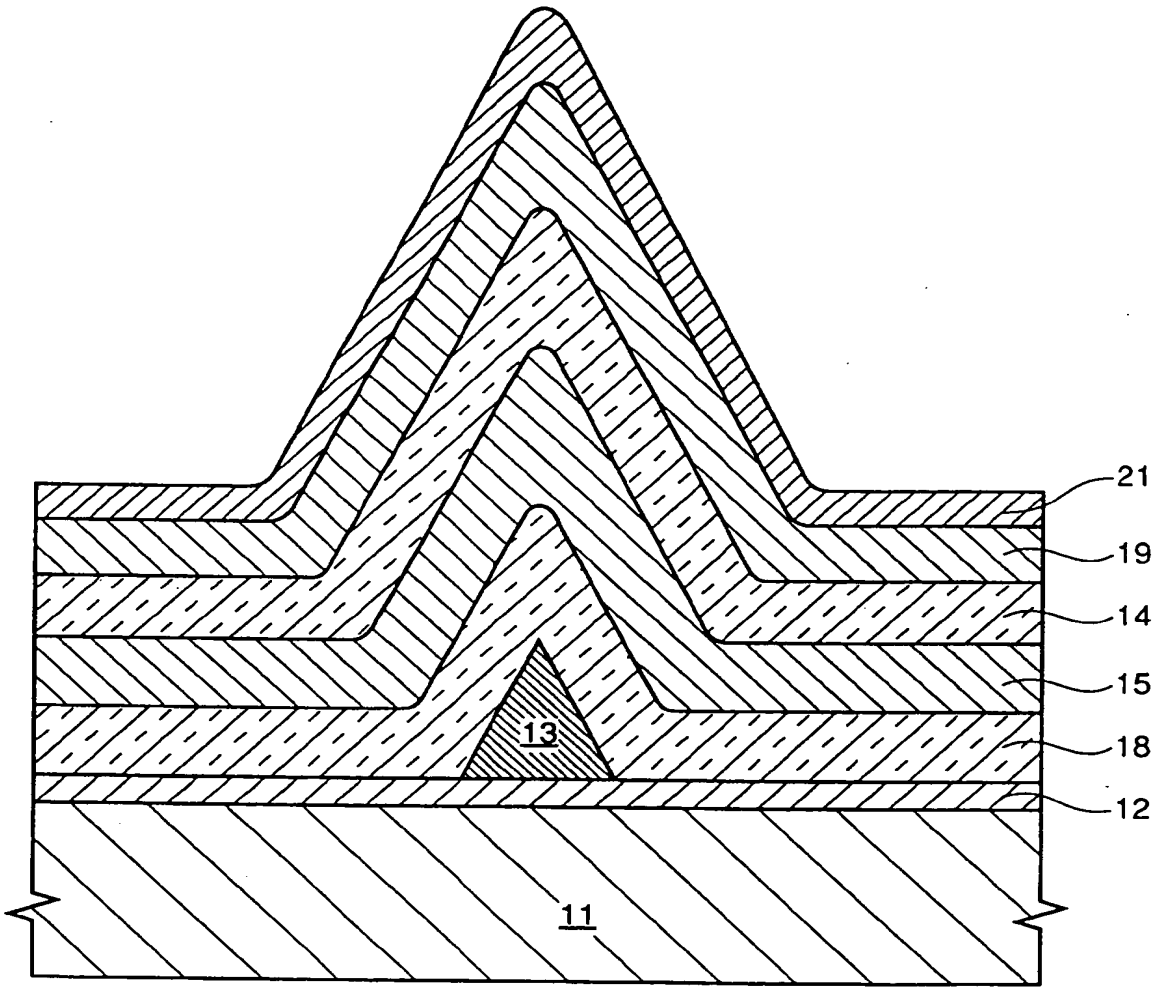

FIG. 3

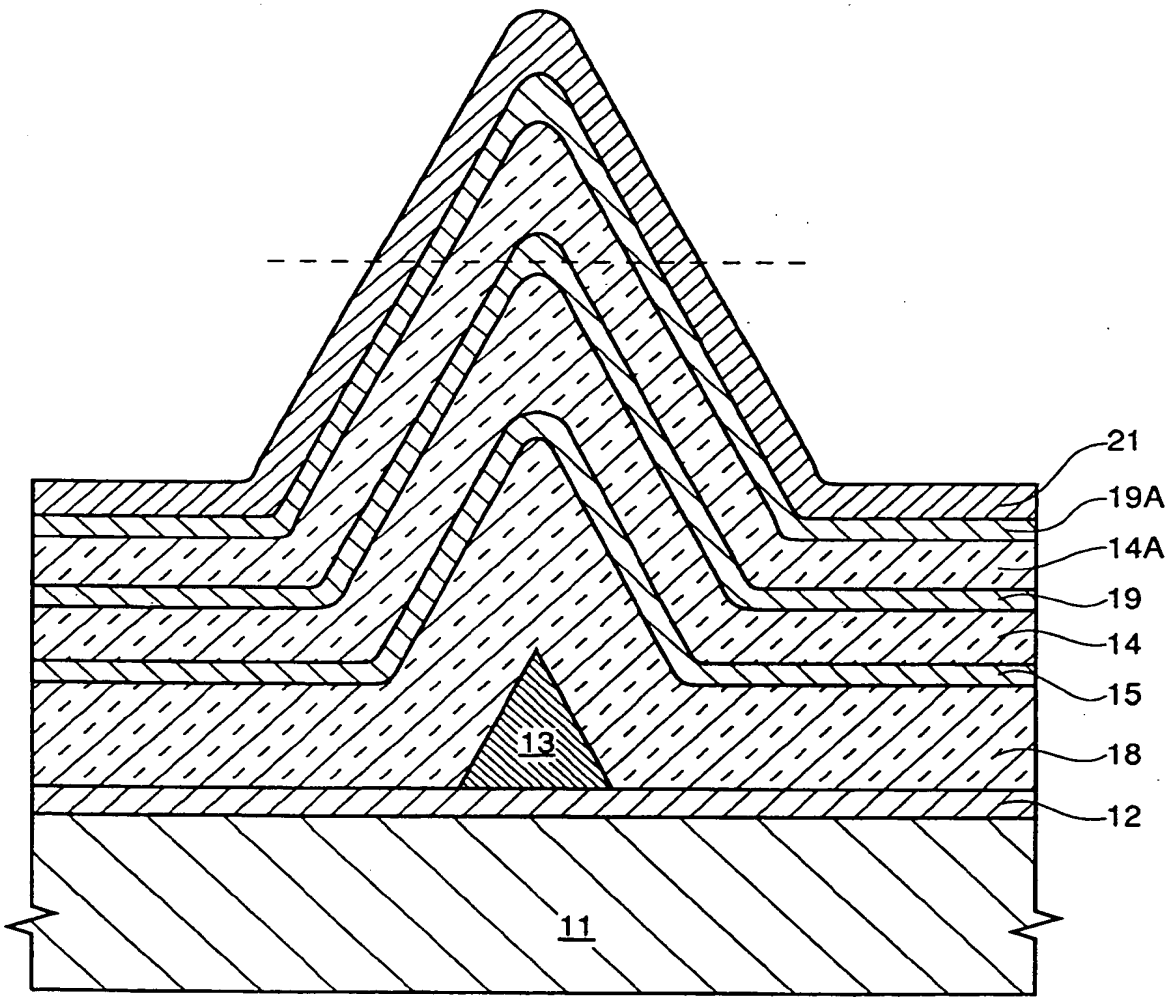

FIG. 3A

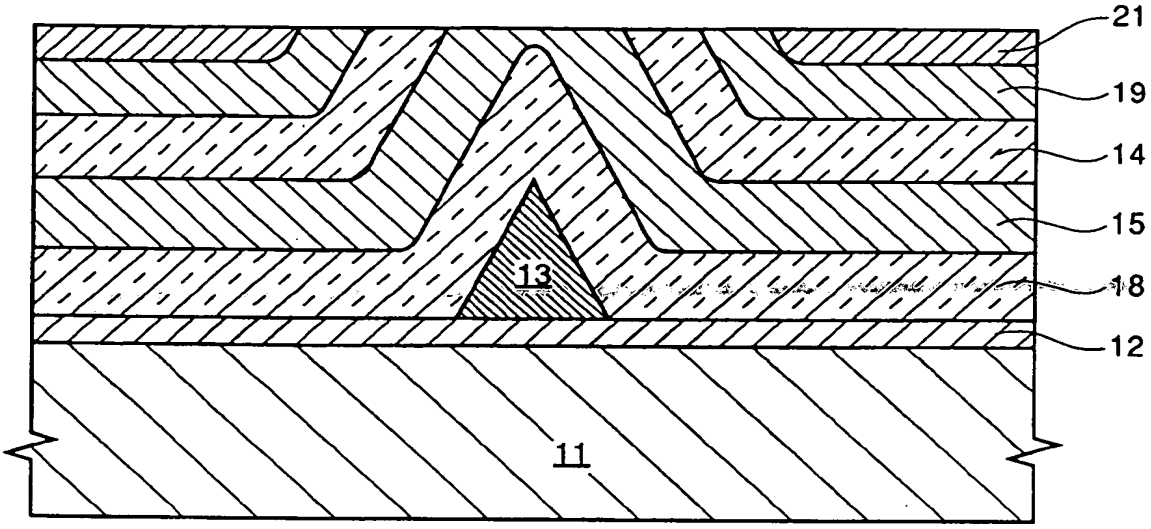

FIG. 4

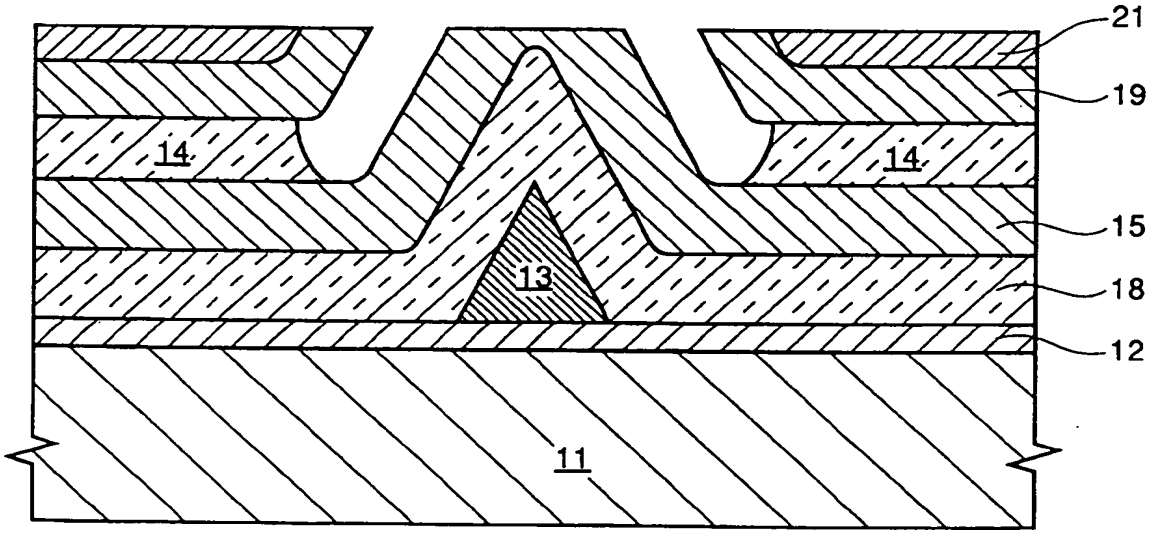

FIG. 5

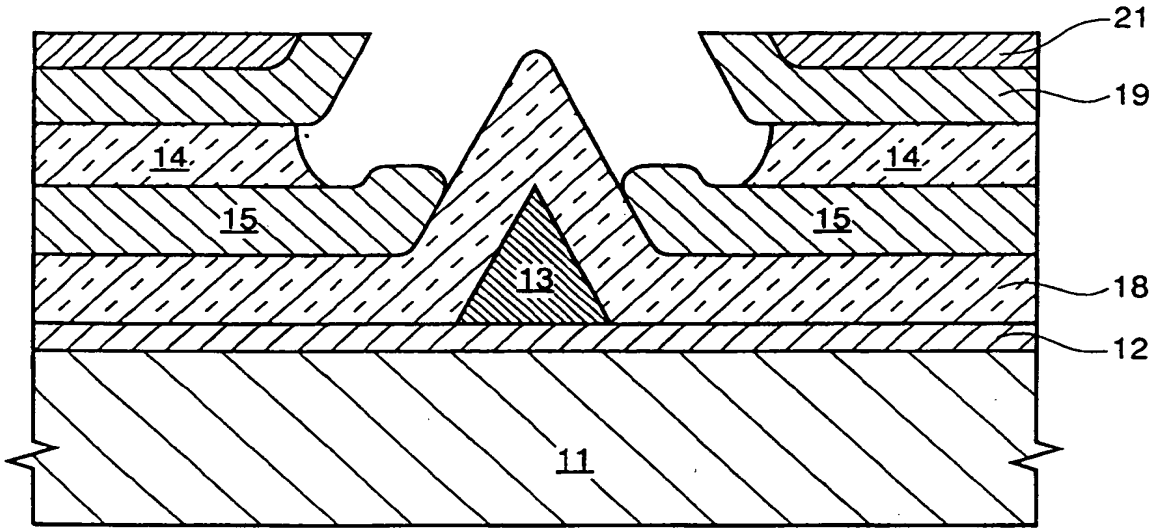

FIG. 6

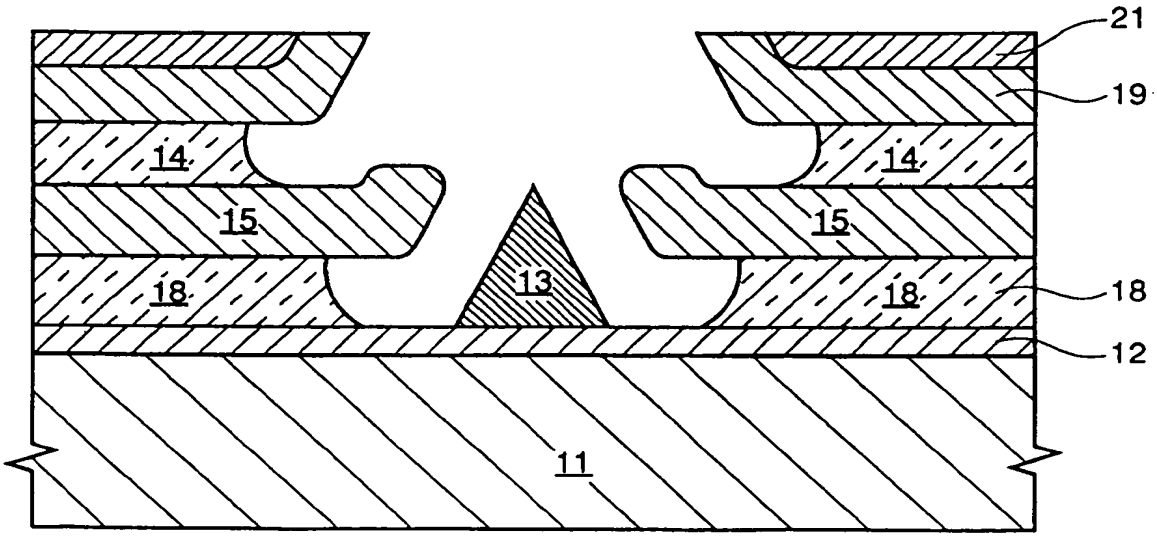

FIG. 7

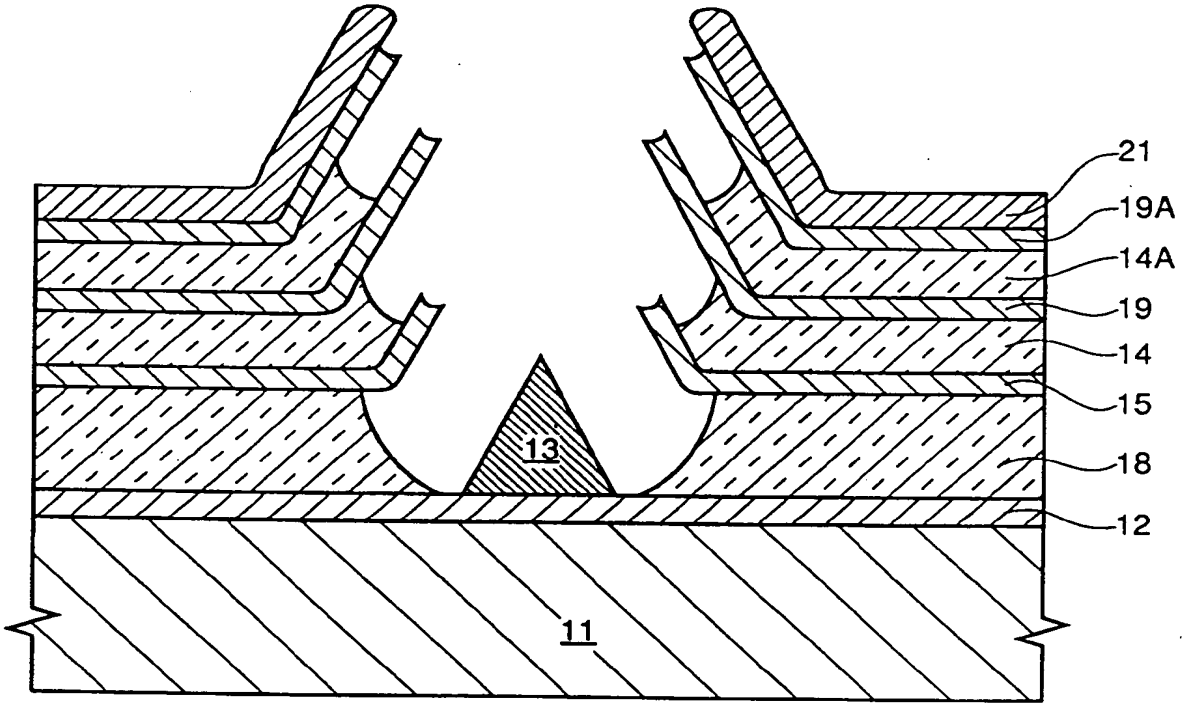

FIG. 7A

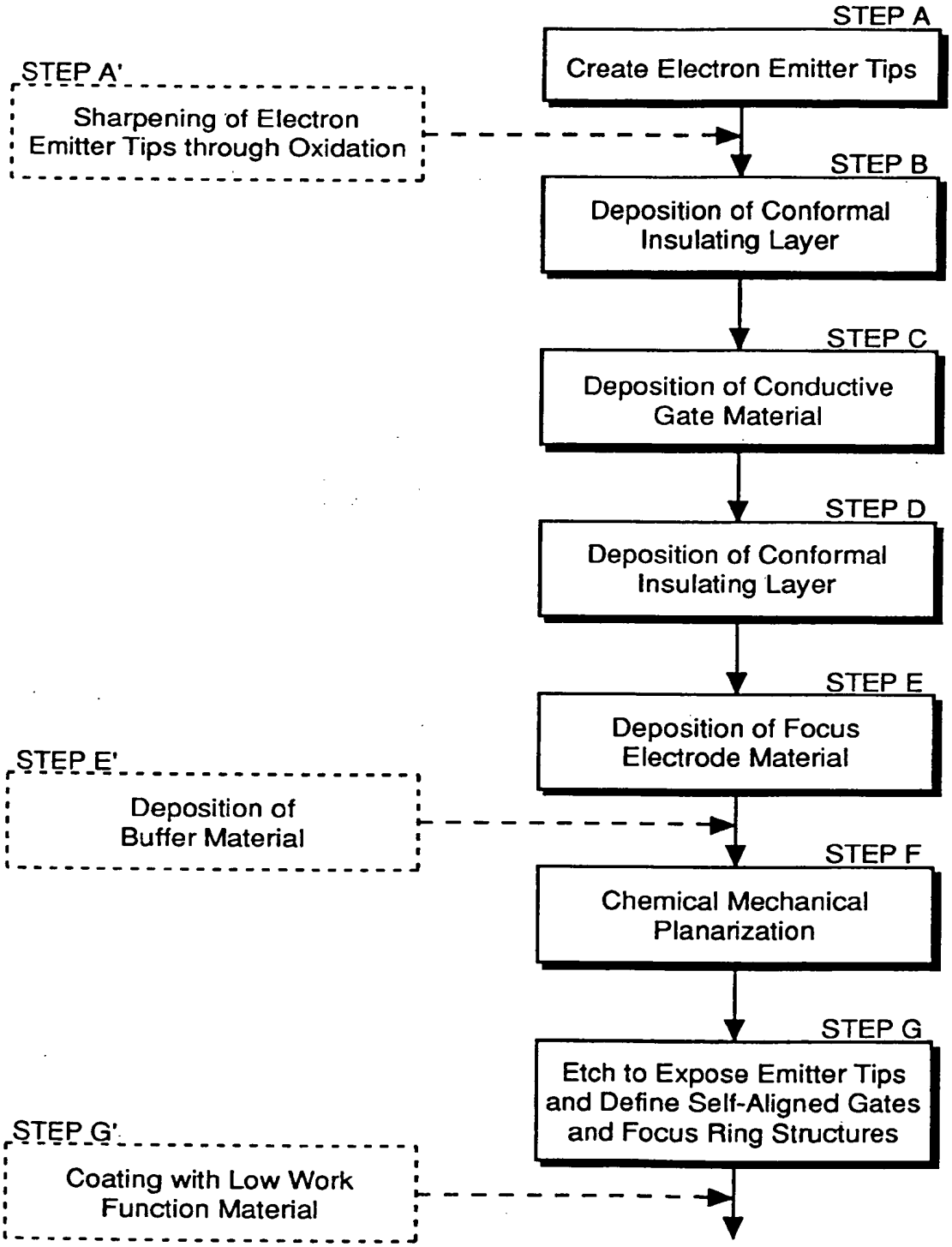
STEP A
Create Electron Emitter Tips
STEP A'
Sharpening of Electron Emitter Tips through Oxidation
STEP B
Deposition of Conformal Insulating Layer
STEP C
Deposition of Conductive Gate Material
STEP D
Deposition of Conformal Insulating Layer
STEP E
Deposition of Focus Electrode Material
STEP E'
Deposition of Buffer Material
STEP F
Chemical Mechanical Planarization
STEP G
Etch to Expose Emitter Tips and Define Self-Aligned Gates and Focus Ring Structures
STEP G'
Coating with Low Work Function Material

FIG. 8

European Patent Office

EUROPEAN SEARCH REPORT

Application Number
EP 93 10 3321

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int. Cl.5)
D,Y	EP-A-0 376 825 (THOMSON TUBES ELECTRONIQUES) * abstract; figures * * column 2, line 50 - column 3, line 2 * * column 2, line 19 - line 24 * * column 4, line 14 - line 16 * * column 4, line 57 - column 5, line 23 * * column 10, line 26 - line 38 *	1,2,7-10	H01J9/02 H01J1/30
Y	US-A-4 671 851 (BEYER ET AL.) * abstract; figures * * column 1, line 42 - line 56 * * column 2, line 51 - line 58 * * column 3, line 57 - column 4, line 4 *	1,2,7-10	
A	US-A-4 964 946 (GRAY ET AL.) * abstract; figures * * column 2, line 42 - line 57 *	1	
D,A	US-A-4 943 343 (BARDAI ET AL.) * figures * * column 1, line 55 - line 58 * * column 2, line 63 - column 3, line 2 * * column 3, line 48 - line 58 *	1	TECHNICAL FIELDS SEARCHED (Int. Cl.5) H01J
D,A	US-A-5 055 158 (GALLAGHER ET AL.) * column 5, line 9 - line 15 * * column 5, line 23 - line 35 *	1	

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	26 MAY 1993	COLVIN G.G.

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
Y : particularly relevant if combined with another document of the same category
A : technological background
O : non-written disclosure
P : intermediate document

T : theory or principle underlying the invention
E : earlier patent document, but published on, or after the filing date
D : document cited in the application
L : document cited for other reasons

& : member of the same patent family, corresponding document

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